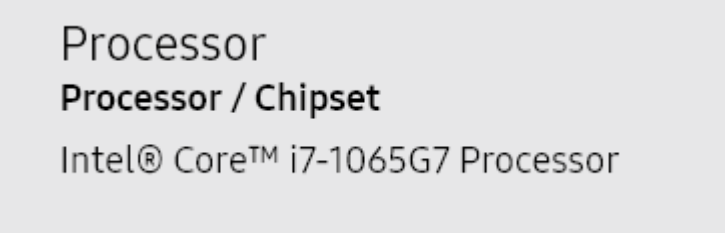
Exhibit 8

U.S. Patent No. 8,193,792 ("'792 Patent")

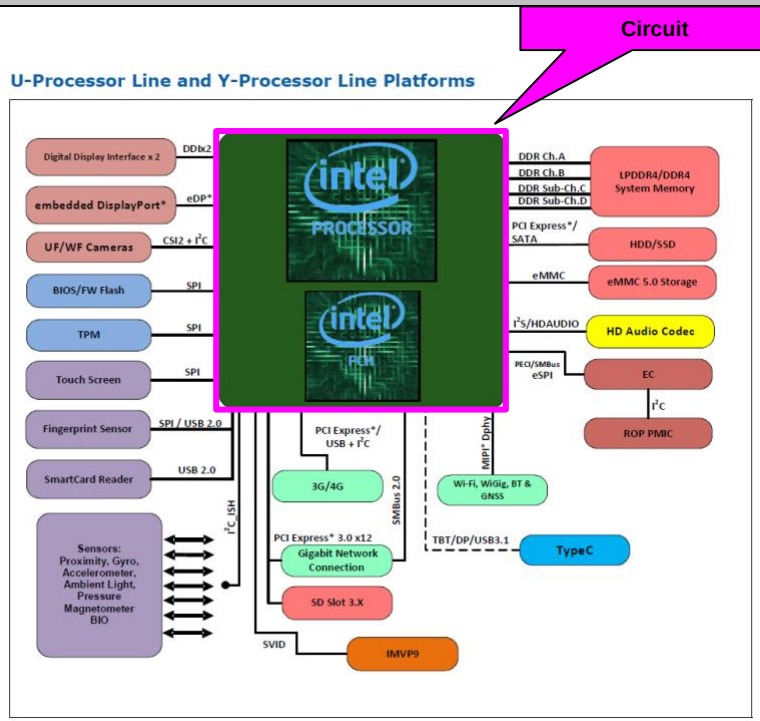
Accused Products

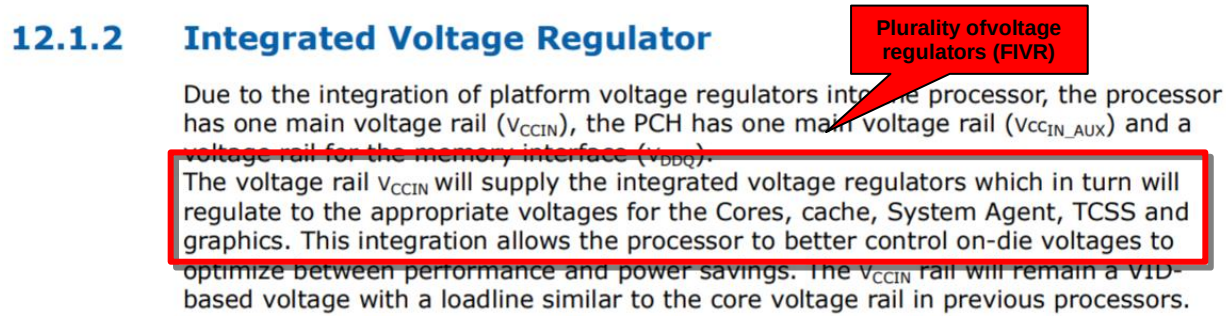
Samsung products with Intel processors featuring Fully Integrated Voltage Regulators, including without limitation the Samsung Galaxy Book Flex 13.3" NP930QCG-K01US ("Accused Products"), infringe at least Claims 1 and 10 of the '792 Patent.

Claim 1

Claim 1	Accused Products
[1pre] A circuit comprising:	To the extent the preamble is limiting, each Accused Product comprises the claimed circuit. For example, the Galaxy Book Flex includes a 10th-generation Intel Core processor, which contains Intel Fully Integrated Voltage Regulator technology. *See, e.g.*:  Screenshot identifying Intel Core i7-1065G7 processor from https://www.samsung.com/us/computing/galaxy-books/galaxy-book-flex/galaxy-book-flex-13-3-qled-512gb-storage-s-pen-included-np930qcg-k01us/

Claim 1	Accused Products
	 Screenshot identifying Intel Core i7-1065G7 as a 10th Generation Core processor (formerly Ice Lake) from https://ark.intel.com/content/www/us/en/ark/products/196597/intel-core-i7-1065g7-processor-8m-cache-up-to-3-90-ghz.html

Claim 1	Accused Products
	 Screenshot, with annotation illustrating the claimed circuit, from https://www.intel.com/content/www/us/en/products/docs/processors/core/10th-gen-core-families-datasheet-vol-1.html
[1a] a first voltage regulator;	Each Accused Product includes a first voltage regulator. For example, the Galaxy Book Flex includes an Intel 10th-generation Core processor featuring Intel's Fully Integrated Voltage Regulator ("FIVR") technology, including a first voltage regulator that provides a supply voltage to the circuit section at a voltage and current level suitable for use by the processor's information processing features ("cores") during operating mode, as explained more fully below. *See, e.g.*:

Claim 1	Accused Products
	 Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, *available at* https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf

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	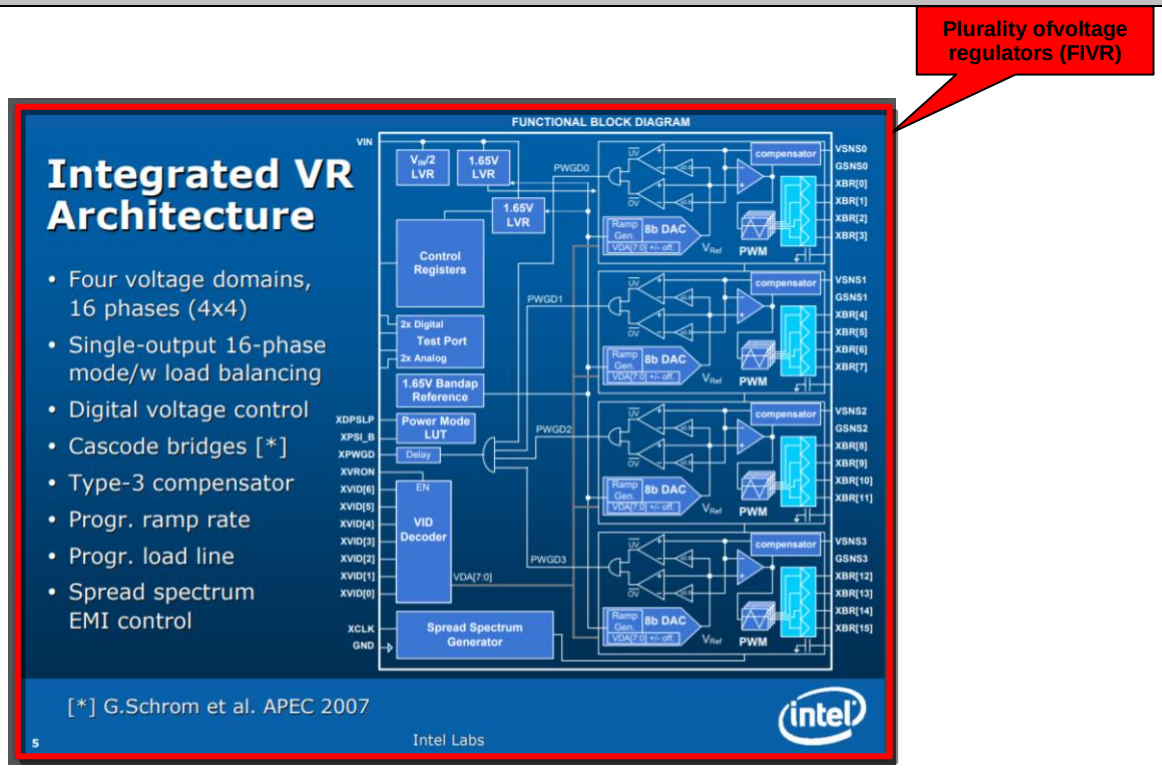 Screenshot, with annotation illustrating the plurality of voltage regulators within the Intel processor, of which one is the first voltage regulator, from https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%E2%80%99s-fully-integrated-coltage-regulator.pdf

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	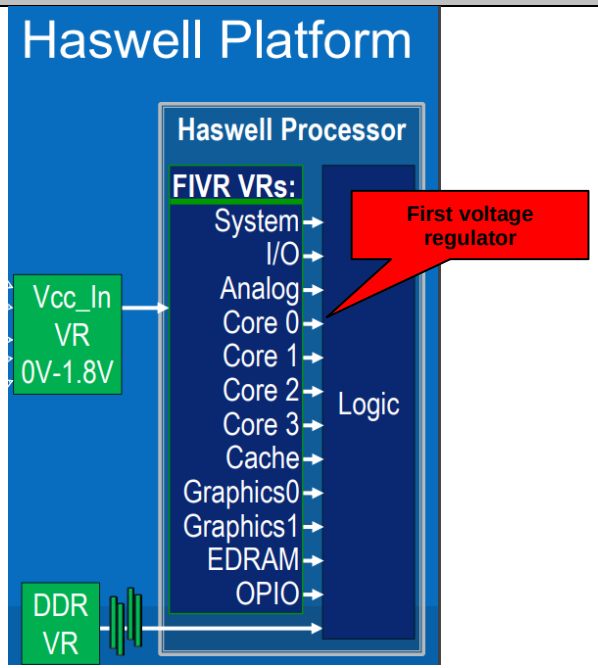 Screenshot, with annotation, from https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%E2%80%99s-fully-integrated-coltage-regulator.pdf

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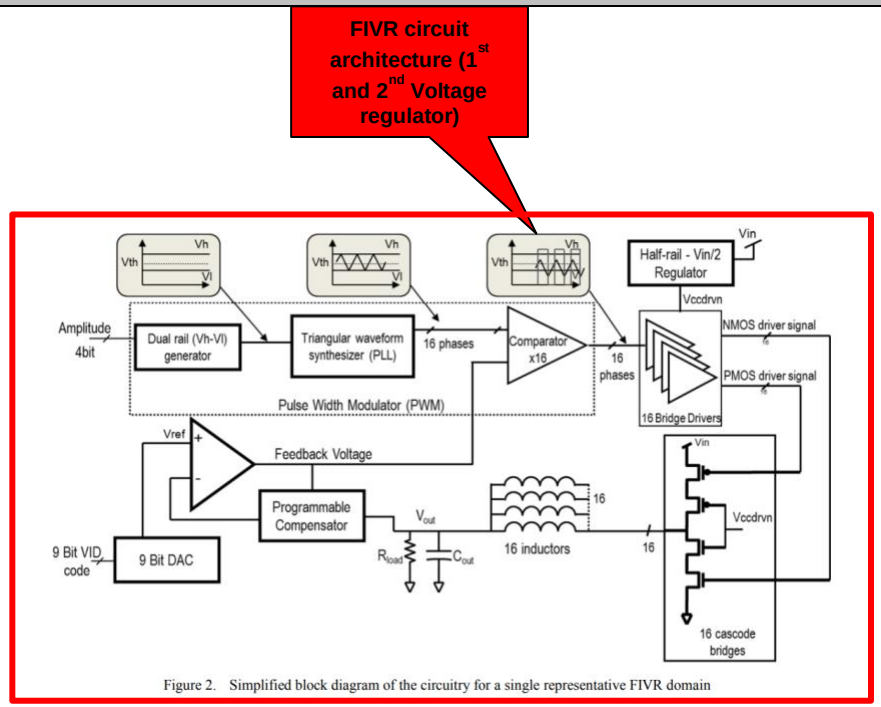
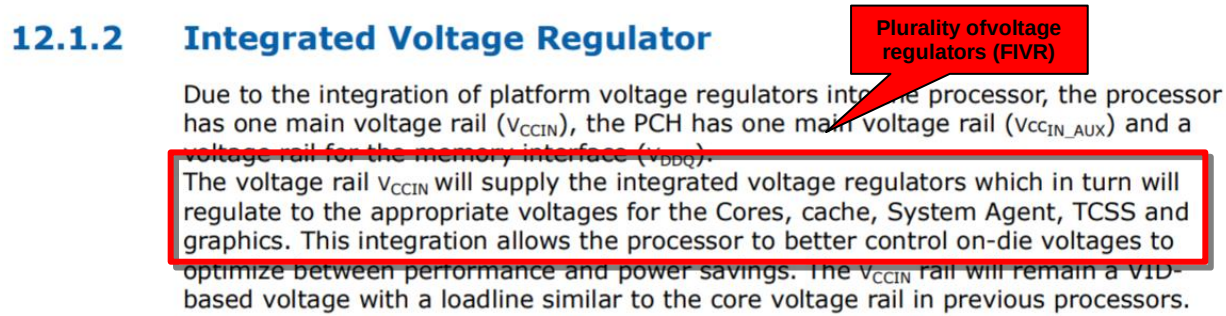
	 Figure 2. Simplified block diagram of the circuitry for a single representative FIVR domain Screenshot, with annotation, from https://www.researchgate.net/publication/271416878_FIVR_-_Fully_integrated_voltage_regulators_on_4th_generation_IntelR_Core_SoCs
[1b] a second voltage regulator; and	Each Accused Product includes a second voltage regulator. For example, the Galaxy Book Flex includes an Intel 10th-generation Core processor featuring Intel's Fully Integrated Voltage Regulator ("FIVR") technology, including a second voltage regulator that provides a standby voltage to the circuit section at a voltage and current level suitable for use by the processor's memory element ("cache") during sleep mode, as explained more fully below. *See, e.g.*:

Claim 1	Accused Products
	 **12.1.2 Integrated Voltage Regulator** Due to the integration of platform voltage regulators into the processor, the processor has one main voltage rail (V_{CCIN}), the PCH has one main voltage rail (Vcc_{IN_AUX}) and a voltage rail for the memory interface (V_{DDQ}). The voltage rail V_{CCIN} will supply the integrated voltage regulators which in turn will regulate to the appropriate voltages for the Cores, cache, System Agent, TCSS and graphics. This integration allows the processor to better control on-die voltages to optimize between performance and power savings. The V_{CCIN} rail will remain a VID-based voltage with a loadline similar to the core voltage rail in previous processors. Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, *available at* https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf

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	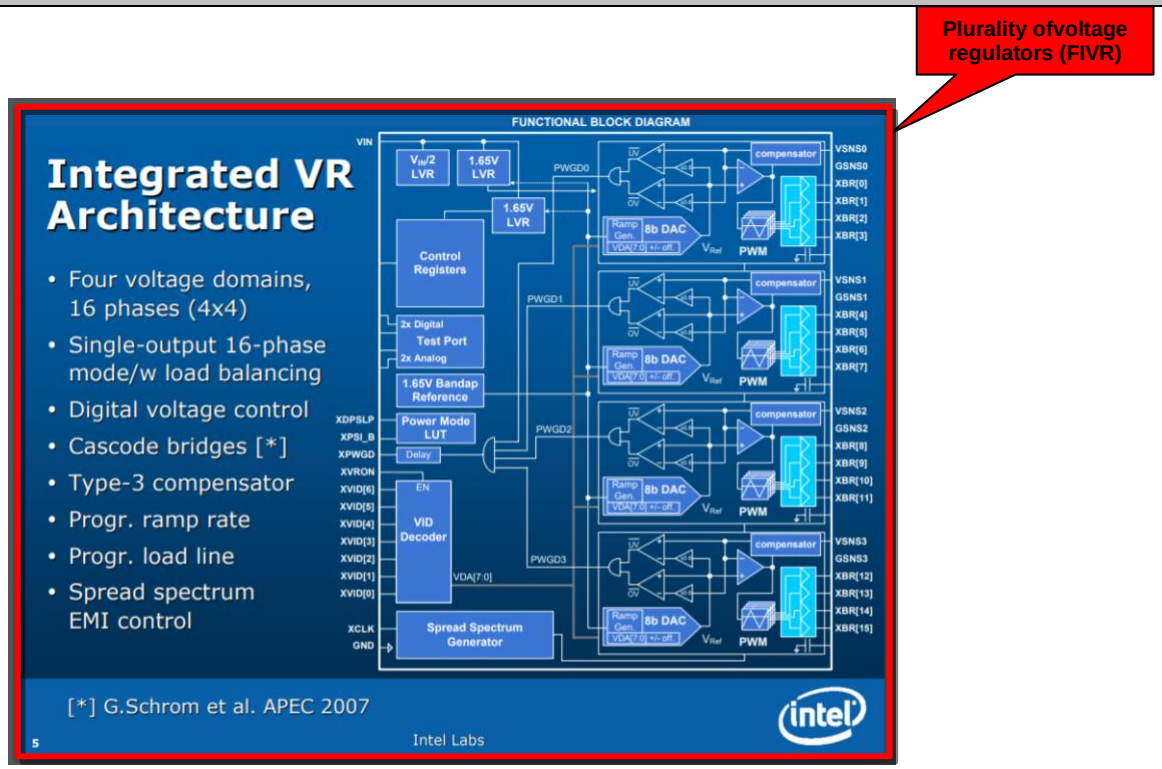 Screenshot, with annotation illustrating the plurality of voltage regulators within the Intel processor, of which one is the second voltage regulator, from https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%E2%80%99s-fully-integrated-coltage-regulator.pdf

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	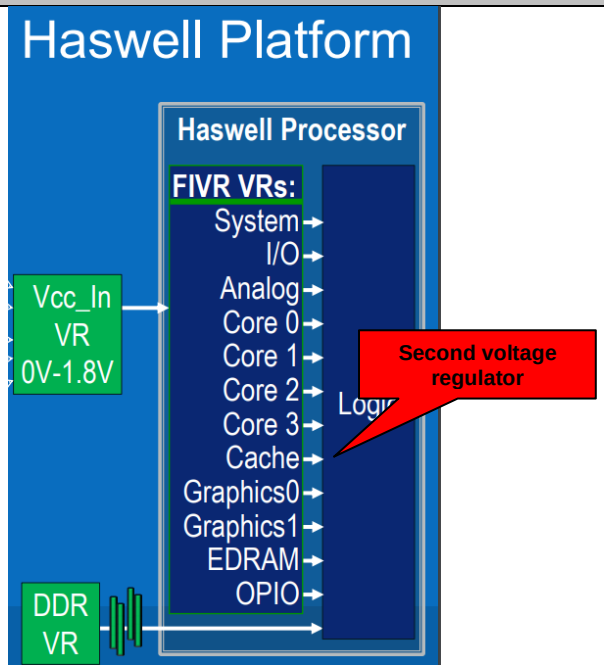 Screenshot, with annotation, from https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%E2%80%99s-fully-integrated-coltage-regulator.pdf

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	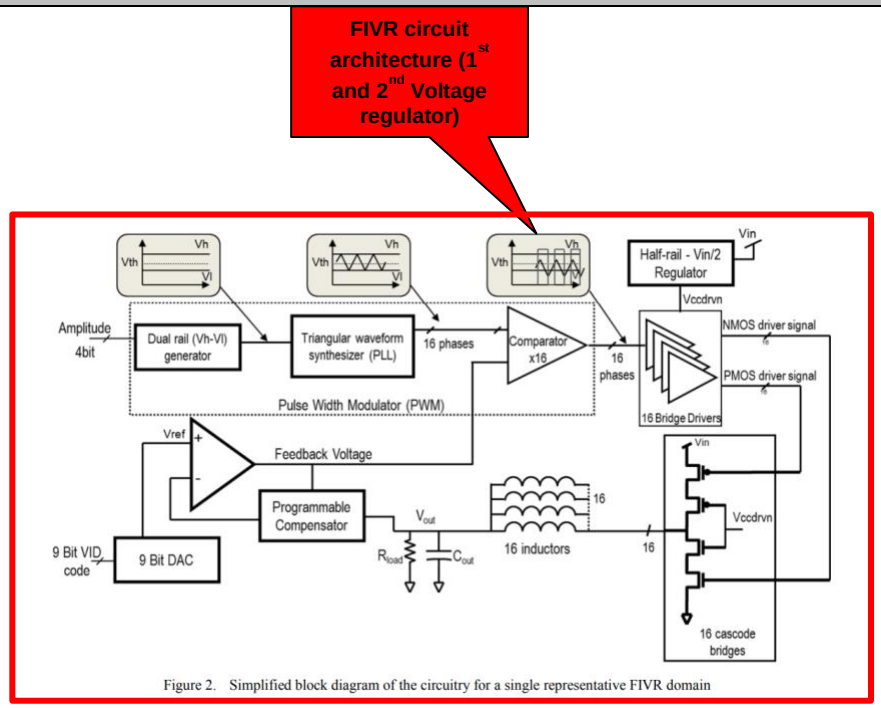 Figure 2. Simplified block diagram of the circuitry for a single representative FIVR domain Screenshot, with annotation, from https://www.researchgate.net/publication/271416878_FIVR_-_Fully_integrated_voltage_regulators_on_4th_generation_IntelR_Core_SoCs
[1c] a circuit section, the circuit section comprising a memory element and operable to:	Each Accused Product includes a circuit section, the circuit section comprising a memory element. For example, the Galaxy Book Flex includes an Intel 10th-generation Core processor featuring a Last Level Cache (“LLC”). The claimed circuit section comprises the LLC, the processor’s information processing unit (cores), and the power control unit. *See, e.g.*:

Claim 1	Accused Products
	2.4.1 Intel® Smart Cache Technology The Intel® Smart Cache Technology is a shared Last Level Cache (LLC). • The LLC may also be referred to as a third level cache. • The LLC is shared between all IA cores as well as the Processor Graphics. • The first and second level caches are not shared between physical cores and each physical core has a separate set of caches. • The size of the LLC is SKU specific with a maximum of 2 MB per physical core and is a 16 way associative cache. Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, *available at* https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf

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	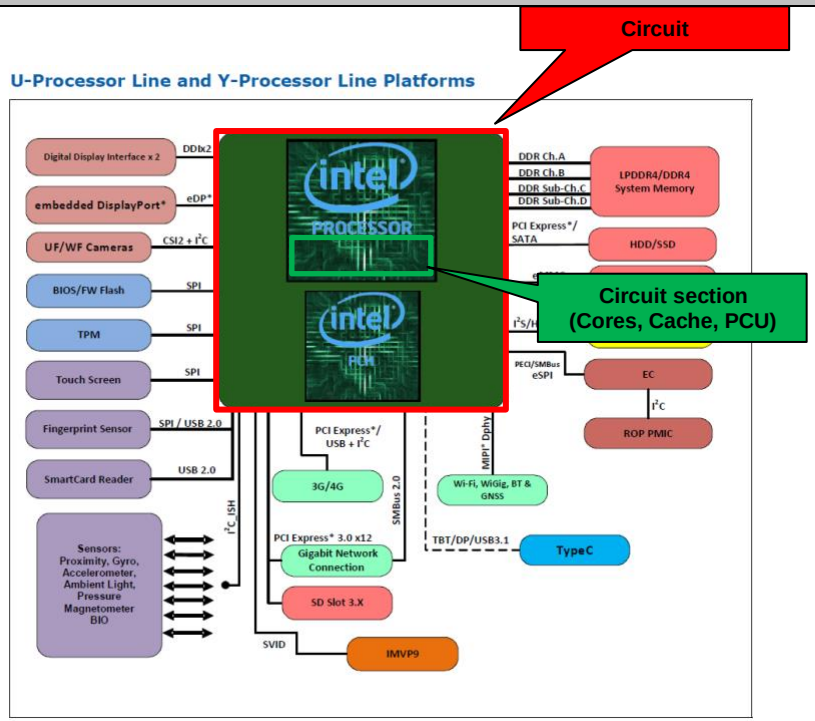 Annotated screenshot showing circuit and circuit section from https://www.intel.com/content/www/us/en/products/docs/processors/core/10th-gen-core-families-datasheet-vol-1.html.
[1d] receive a supply voltage from the first voltage regulator when in an operating mode;	In each Accused Product, the circuit section is operable to receive a supply voltage from the first voltage regulator when in an operating mode. For example, the Galaxy Book Flex receives a certain core voltage from the first voltage regulator while in an operating mode, such as a C0 state ("The normal operating state of a processor IA core where code is being executed"). *See, e.g.*:

Claim 1	Accused Products
	operating mode Table 3-4. Core C-states Core C-State / C-State Request Instruction / Description C0 / N/A / The normal operating state of a processor IA core where code is being executed Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, *available at* https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf

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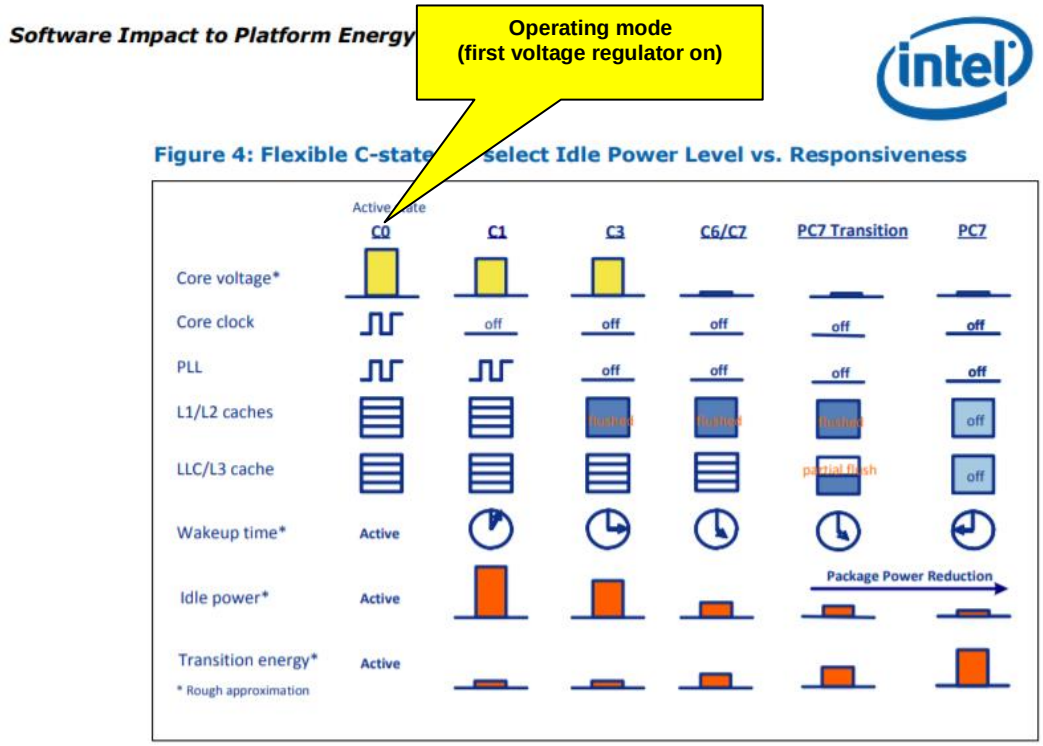
	 Annotated screenshot from https://www.intel.ru/content/dam/doc/white-paper/energy-efficient-platforms-2011-white-paper.pdf
[1e] transition from the operating mode to a sleep mode, the transition comprising deactivation of inputs of the circuit section; and	In each Accused Product, the circuit section is operable to transition from the operating mode to a sleep mode, the transition comprising deactivation of inputs of the circuit section. For example, the Intel processor in the Galaxy Book Flex can transition into a sleep mode, such as the C6 state, in which the information processor units flush their L1 instruction/data caches and L2 caches, save their architectural state, deactivate their inputs, and deactivate the first voltage regulator.

Claim 1	Accused Products
	See, e.g.:

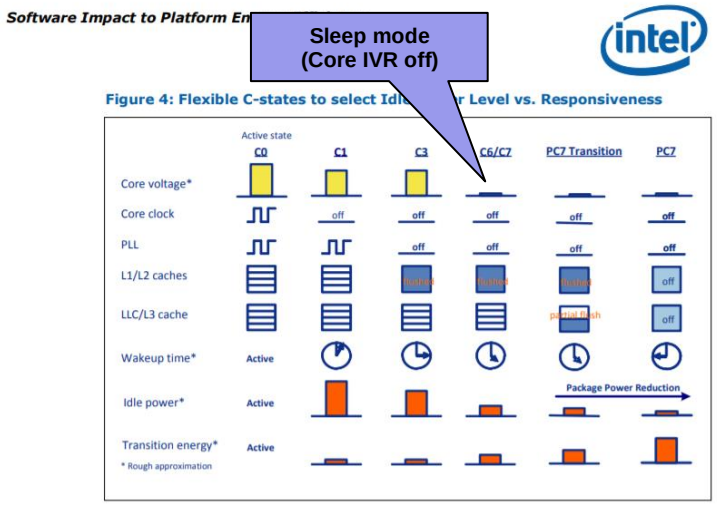
Table 3-4. Core C-states

Core C-State	C-State Request Instruction	Description
C0	N/A	The normal … executed … being
C1	MWAIT(C1)	AutoHalt - … (package in C0 state)
C1E	MWAIT(C1E)	Core C1 + lowest frequency and voltage … ating point (package in C0 state)
C6-C10	MWAIT(C6/7/7s/ C8/9/10) or IO read=P_LVL3/4/5/ 6/7/8	Processor IA, flush their L1 instruction cache, L1 data cache, and L2 cache to the LLC shared cache cores save their architectural state to a SRAM before reducing IA cores voltage, if possible may also be reduced to 0V. Core clocks are off.

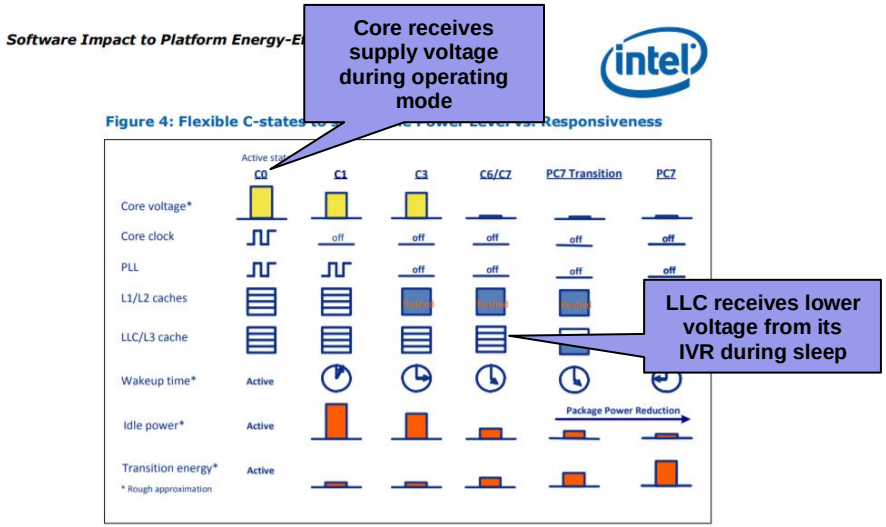
Sleep mode

deactivation of inputs

Excerpt from 10th Gen Intel Core Processor Families Datasheet, Vol. 1, *available at* https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/10th-gen-core-families-datasheet-vol-1-datasheet.pdf



Illustrated screenshot from https://www.intel.ru/content/dam/doc/white-paper/energy-efficient-platforms-2011-white-paper.pdf

Claim 1	Accused Products
[1f] receive a standby voltage from the second voltage regulator when in the sleep mode, the standby voltage being less than the supply voltage and sufficient to preserve an information item stored in the memory element.	In each Accused Product, the circuit section is operable to receive a standby voltage from the second voltage regulator when in the sleep mode, the standby voltage being less than the supply voltage and sufficient to preserve an information item stored in the memory element. For example, the Intel processor in the Galaxy Book Flex continues to operate the integrated voltage regulator associated with the Last Level Cache during sleep mode (such as the C6 core state) in order to receive a lower voltage sufficient to preserve the contents of the LLC memory. *See, e.g.*  Illustrated screenshot from https://www.intel.ru/content/dam/doc/white-paper/energy-efficient-platforms-2011-white-paper.pdf

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	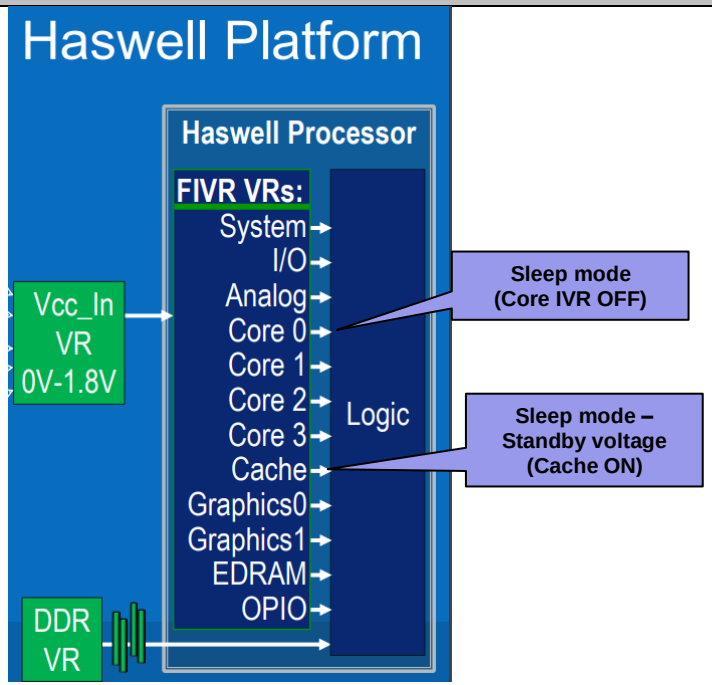 Illustrated screenshot from https://www.psma.com/sites/default/files/uploads/tech-forums-packaging/presentations/is87-package-and-platform-view-intel%E2%80%99s-fully-integrated-coltage-regulator.pdf

Claim 10

Claim 10	Accused Products
[10pre] A method comprising:	To the extent the preamble is limiting, each Accused Product performs the claimed method. *See supra* claim element [1pre].
[10a] delivering to a circuit section of a circuit a supply voltage from a first voltage	Each Accused Product performs delivering to a circuit section of a circuit a supply voltage from a first voltage regulator when in an operating mode.

Claim 10	Accused Products
regulator when in an operating mode;	*See supra* claim element [1d].
[10b] transitioning from the operating mode to a sleep mode, the transition comprising deactivation of inputs of the circuit section; and	Each Accused Product performs transitioning from the operating mode to a sleep mode, the transition comprising deactivation of inputs of the circuit section. *See supra* claim element [1e].
[10c] delivering to the circuit section a standby voltage from a second voltage regulator when in the sleep mode, the standby voltage being less than the supply voltage and sufficient to preserve an information item stored in a memory element.	Each Accused Product performs delivering to the circuit section a standby voltage from a second voltage regulator when in the sleep mode, the standby voltage being less than the supply voltage and sufficient to preserve an information item stored in a memory element. *See supra* claim element [1f].